MCP6S21/2/6/8

Single-Ended, Rail-to-Rail I/O, Low Gain PGA

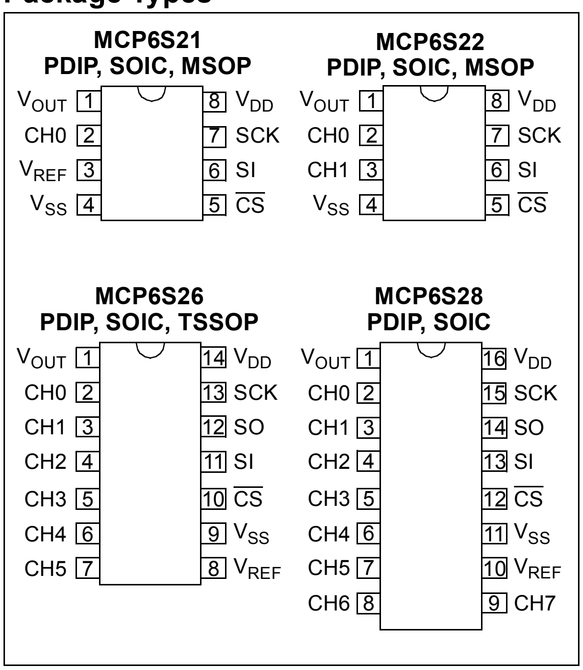
Features

- Multiplexed Inputs: 1, 2, 6 or 8 channels
- 8 Gain Selections:
  - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI™)
- Rail-to-Rail Input and Output
- Low Gain Error: ±1% (max)
- Low Offset: ±275 µV (max)
- High Bandwidth: 2 to 12 MHz (typ)
- Low Noise: 10 nV/√Hz @ 10 kHz (typ)
- Low Supply Current: 1.0 mA (typ)
- Single Supply: 2.5V to 5.5V

Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

Package Types

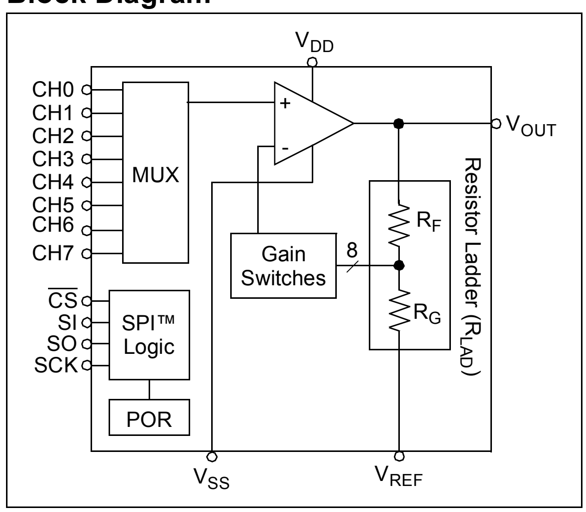


Description

The Microchip Technology Inc. MCP6S21/2/6/8 are analog Programmable Gain Amplifiers (PGA). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to eight channels through an SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single supply applications needing flexible performance or multiple inputs.

The one channel MCP6S21 and the two channel MCP6S22 are available in 8-pin PDIP, SOIC and MSOP packages. The six channel MCP6S26 is available in 14-pin PDIP, SOIC and TSSOP packages. The eight channel MCP6S28 is available in 16-pin PDIP and SOIC packages. All parts are fully specified from -40°C to +85°C.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
All inputs and outputs....................... V_{SS} - 0.3V to V_{DD} +0.3V
Difference Input voltage .... $|V_{DD} - V_{SS}|$
Output Short Circuit Current..................................continuous
Current at Input Pin ....±2 mA
Current at Output and Supply Pins ....±30 mA
Storage temperature ....-65°C to +150°C
Junction temperature ....+150°C
ESD protection on all pins (HBM;MM)................. ≥ 2 kV; 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{OUT}	Analog Output
CH0-CH7	Analog Inputs
V_{SS}	Negative Power Supply
V_{DD}	Positive Power Supply
SCK	SPI Clock Input
SI	SPI Serial Data Input
SO	SPI Serial Data Output
$\overline{CS}$	SPI Chip Select
V_{REF}	External Reference Pin

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Amplifier Input						
Input Offset Voltage	V_{OS}	-275	—	+275	µV	G = +1, V_{DD} = 4.0V
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	±4	—	µV/°C	T_A = -40 to +85°C
Power Supply Rejection Ratio	PSRR	70	85	—	dB	G = +1 **(Note 1)**
Input Bias Current	I_B	—	±1	—	pA	CHx = V_{DD}/2
Input Bias Current over Temperature	I_B	—	—	250	pA	T_A = -40 to +85°C, CHx = V_{DD}/2
Input Impedance	Z_{IN}	—	10^{13}‖15	—	Ω‖pF	
Input Voltage Range	V_{IVR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Amplifier Gain						
Nominal Gains	G	—	1 to 32	—	V/V	+1, +2, +4, +5, +8, +10, +16 or +32
DC Gain Error G = +1	g_E	-0.1	—	+0.1	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
G ≥ +2	g_E	-1.0	—	+1.0	%	V_{OUT} ≈ 0.3V to V_{DD} – 0.3V
DC Gain Drift G = +1	$\Delta G/\Delta T_A$	—	±0.0002	—	%/°C	T_A = -40 to +85°C
G ≥ +2	$\Delta G/\Delta T_A$	—	±0.0004	—	%/°C	T_A = -40 to +85°C
Internal Resistance	R_{LAD}	3.4	4.9	6.4	kΩ	**(Note 1)**
Internal Resistance over Temperature	$\Delta R_{LAD}/\Delta T_A$	—	+0.028	—	%/°C	**(Note 1)** T_A = -40 to +85°C
Amplifier Output						
DC Output Non-linearity G = +1	V_{ONL}	—	±0.003	—	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
G ≥ +2	V_{ONL}	—	±0.001	—	% of FSR	V_{OUT} = 0.3V to V_{DD} – 0.3V, V_{DD} = 5.0V
Maximum Output Voltage Swing	V_{OH}, V_{OL}	V_{SS}+20	—	V_{DD}-100	mV	G ≥ +2; 0.5V output overdrive
		V_{SS}+60	—	V_{DD}-60		G ≥ +2; 0.5V output overdrive, V_{REF} = V_{DD}/2
Short-Circuit Current	$I_{O(SC)}$	—	±30	—	mA	

Note 1: R_{LAD} (R_F + R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S22 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

3: The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to $V_{DD}/2$, SI and SCK are tied low and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current	I_Q	0.5	1.0	1.35	mA	I_O = 0 **(Note 2)**
Quiescent Current, Shutdown mode	I_{Q_SHDN}	—	0.5	1.0	µA	I_O = 0 **(Note 2)**
Power-On Reset						
POR Trip Voltage	V_{POR}	1.2	1.7	2.2	V	**(Note 3)**
POR Trip Voltage Drift	$\Delta V_{POR}/\Delta T$	—	-3.0	—	mV/°C	T_A = -40°C to+85°C

Note 1: R_{LAD} (R_F + R_G in Figure 4-1) connects V_{REF}, V_{OUT} and the inverting input of the internal amplifier. The MCP6S22 has V_{REF} tied internally to V_{SS}, so V_{SS} is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's V_{SS} pin be tied directly to ground to avoid noise problems.

2: I_Q includes current in R_{LAD} (typically 60 µA at V_{OUT} = 0.3V). Both I_Q and I_{Q_SHDN} exclude digital switching currents.

3: The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 =(0.3V)/G, CH1 to CH7=0.3V, R_L = 10 kΩ to $V_{DD}/2$, C_L = 60 pF, SI and SCK are tied low, and $\overline{CS}$ is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
-3 dB Bandwidth	BW	—	2 to 12	—	MHz	All gains; V_{OUT} < 100 mV_{P-P} **(Note 1)**
Gain Peaking	GPK	—	0	—	dB	All gains; V_{OUT} < 100 mV_{P-P}
Total Harmonic Distortion plus Noise						
f = 1 kHz, G = +1 V/V	THD+N	—	0.0015	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +4 V/V	THD+N	—	0.0058	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 22 kHz
f = 1 kHz, G = +16 V/V	THD+N	—	0.023	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 22 kHz
f = 20 kHz, G = +1 V/V	THD+N	—	0.0035	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +4 V/V	THD+N	—	0.0093	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
f = 20 kHz, G = +16 V/V	THD+N	—	0.036	—	%	V_{OUT} = 1.5V ± $1.0V_{PK}$, V_{DD} = 5.0V, BW = 80 kHz
Step Response						
Slew Rate	SR	—	4.0	—	V/µs	G = 1, 2
		—	11	—	V/µs	G = 4, 5, 8, 10
		—	22	—	V/µs	G = 16, 32
Noise						
Input Noise Voltage	E_{ni}	—	3.2	—	μV_{P-P}	f = 0.1 Hz to 10 kHz **(Note 2)**
		—	26	—		f = 0.1 Hz to 200 kHz **(Note 2)**
Input Noise Voltage Density	e_{ni}	—	10	—	nV/√Hz	f = 10 kHz **(Note 2)**
Input Noise Current Density	i_{ni}	—	4	—	fA/√Hz	f = 10 kHz

Note 1: See Table 4-1 for a list of typical numbers.

2: E_{ni} and e_{ni} include ladder resistance noise. See Figure 2-33 for e_{ni} vs. G data.

DIGITAL CHARACTERISTICS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{REF} = V_{SS}, G = +1 V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V, R_L = 10 kΩ to V_{DD}/2, C_L = 60 pF, SI and SCK are tied low, and $\overline{CS}$ is tied high.						
SPI Inputs ($\overline{CS}$, SI, SCK)						
Logic Threshold, Low	V_{IL}	0	—	$0.3V_{DD}$	V	
Input Leakage Current	I_{IL}	-1.0	—	+1.0	µA	
Logic Threshold, High	V_{IH}	$0.7V_{DD}$	—	V_{DD}	V	
Amplifier Output Leakage Current	—	-1.0	—	+1.0	µA	In Shutdown mode
SPI Output (SO, for MCP6S26 and MCP6S28)						
Logic Threshold, Low	V_{OL}	V_{SS}	—	V_{SS}+0.4	V	I_{OL} = 2.1 mA, V_{DD} = 5V
Logic Threshold, High	V_{OH}	V_{DD}-0.5	—	V_{DD}	V	I_{OH} = -400 µA
SPI Timing						
Pin Capacitance	C_{PIN}	—	10	—	pF	All digital I/O pins
Input Rise/Fall Times ($\overline{CS}$, SI, SCK)	t_{RFI}	—	—	2	µs	**Note 1**
Output Rise/Fall Times (SO)	t_{RFO}	—	5	—	ns	MCP6S26 and MCP6S28
$\overline{CS}$ high time	t_{CSH}	40	—	—	ns	
SCK edge to $\overline{CS}$ fall setup time	t_{CS0}	10	—	—	ns	SCK edge when $\overline{CS}$ is high
$\overline{CS}$ fall to first SCK edge setup time	t_{CSSC}	40	—	—	ns	
SCK Frequency	f_{SCK}	—	—	10	MHz	V_{DD} = 5V **(Note 2)**
SCK high time	t_{HI}	40	—	—	ns	
SCK low time	t_{LO}	40	—	—	ns	
SCK last edge to $\overline{CS}$ rise setup time	t_{SCCS}	30	—	—	ns	
$\overline{CS}$ rise to SCK edge setup time	t_{CS1}	100	—	—	ns	SCK edge when $\overline{CS}$ is high
SI set-up time	t_{SU}	40	—	—	ns	
SI hold time	t_{HD}	10	—	—	ns	
SCK to SO valid propagation delay	t_{DO}	—	—	80	ns	MCP6S26 and MCP6S28
$\overline{CS}$ rise to SO forced to zero	t_{SOZ}	—	—	80	ns	MCP6S26 and MCP6S28
Channel and Gain Select Timing						
Channel Select Time	t_{CH}	—	1.5	—	µs	CHx = 0.6V, CHy =0.3V, G = 1, CHx to CHy select $\overline{CS}$ = $0.7V_{DD}$ to V_{OUT} 90% point
Gain Select Time	t_G	—	1	—	µs	CHx = 0.3V, G = 5 to G = 1 select, $\overline{CS}$ = $0.7V_{DD}$ to V_{OUT} 90% point
Shutdown Mode Timing						
Out of Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output Turn-on Time	t_{ON}	—	3.5	10	µs	$\overline{CS}$ = $0.7V_{DD}$ to V_{OUT} 90% point
Into Shutdown mode ($\overline{CS}$ goes high) to Amplifier Output High-Z Turn-off Time	t_{OFF}	—	1.5	—	µs	$\overline{CS}$ = $0.7V_{DD}$ to V_{OUT} 90% point
POR Timing						
Power-On Reset power-up time	t_{RPU}	—	30	—	µs	V_{DD} = V_{POR} - 0.1V to V_{POR} + 0.1V, 50% V_{DD} to 90% V_{OUT} point
Power-On Reset power-down time	t_{RPD}	—	10	—	µs	V_{DD} = V_{POR} + 0.1V to V_{POR} - 0.1V, 50% V_{DD} to 90% V_{OUT} point

Note 1: Not tested in production. Set by design and characterization.

2: When using the device in the daisy chain configuration, maximum clock frequency is determined by a combination of propagation delay time ($t_{DO} \le 80$ ns), data input setup time ($t_{SU} \ge 40$ ns), SCK high time ($t_{HI} \ge 40$ ns), and SCK rise and fall times of 5 ns. Maximum f_{SCK} is, therefore, ≈ 5.8 MHz.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.5V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note Note:)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 16L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 16L-SOIC	θ_{JA}	—	90	—	°C/W	

Note 1: The MCP6S21/2/6/8 family of PGAs operates over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature (150°C).

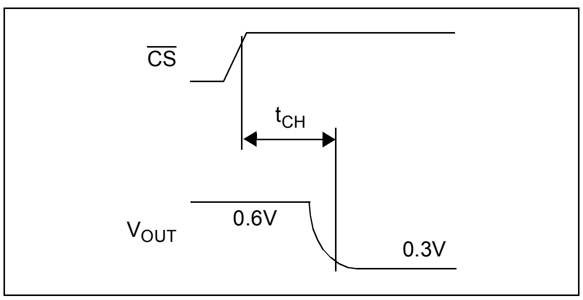


FIGURE 1-1: *Channel Select Timing Diagram.*

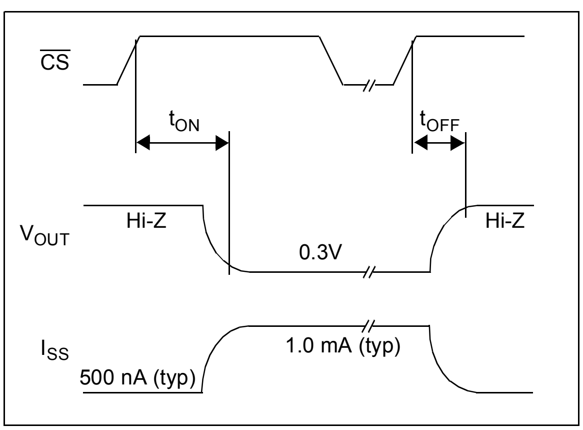


FIGURE 1-2: *PGA Shutdown timing diagram (must enter correct commands before $\overline{CS}$ goes high).*

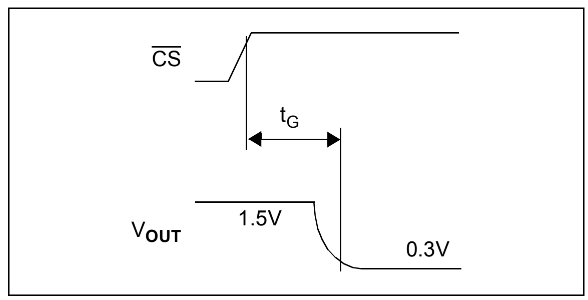


FIGURE 1-3: *Gain Select Timing Diagram.*

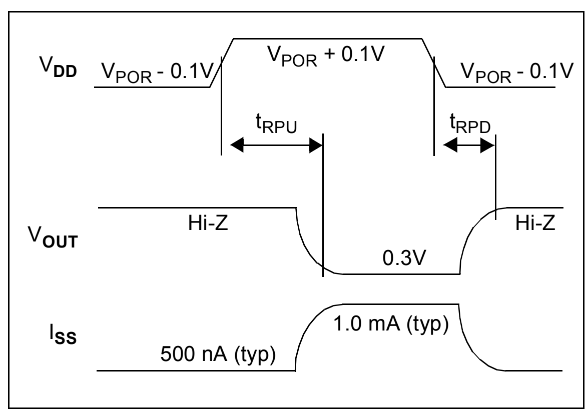
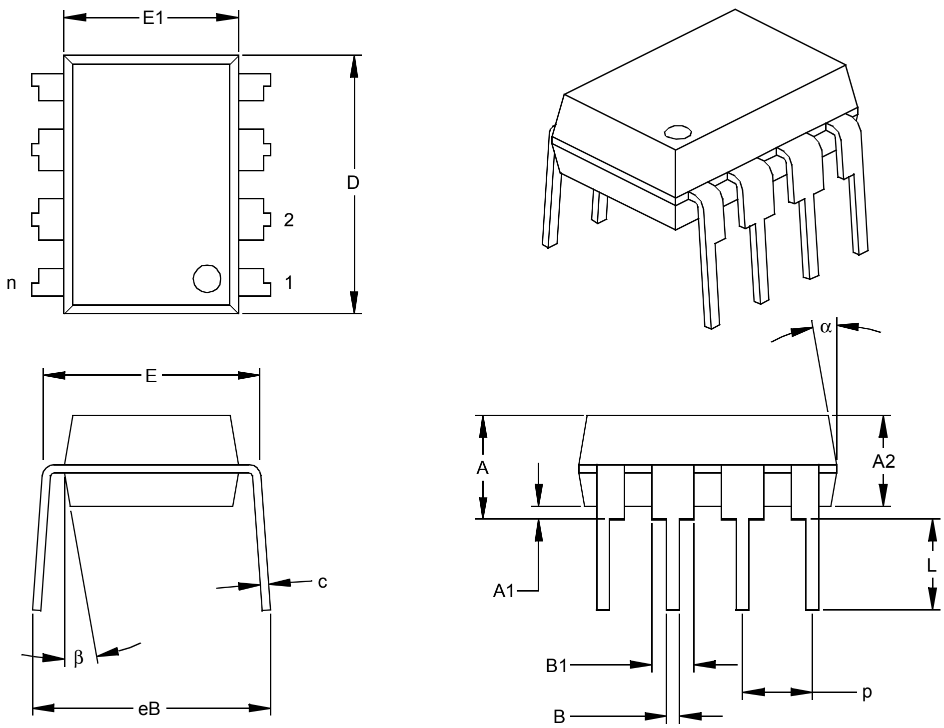


FIGURE 1-4: *POR power-up and power-down timing diagram.*

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP6S21:	One Channel PGA
	MCP6S21T:	One Channel PGA (Tape and Reel for SOIC and MSOP)
	MCP6S22:	Two Channel PGA
	MCP6S22T:	Two Channel PGA (Tape and Reel for SOIC and MSOP)
	MCP6S26:	Six Channel PGA
	MCP6S26T:	Six Channel PGA (Tape and Reel for SOIC and TSSOP)
	MCP6S28:	Eight Channel PGA
	MCP6S28T:	Eight Channel PGA (Tape and Reel for SOIC)
Temperature Range:	I	= -40°C to +85°C
Package:	MS	= Plastic Micro Small Outline (MSOP), 8-lead
	P	= Plastic DIP (300 mil Body), 8, 14, and 16-lead
	SN	= Plastic SOIC, (150 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14, 16-lead
	ST	= Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a) MCP6S21-I/P: One Channel PGA, PDIP package.

b) MCP6S21-I/SN: One Channel PGA, SOIC package.

c) MCP6S21-I/MS: One Channel PGA, MSOP package.

d) MCP6S22-I/MS: Two Channel PGA, MSOP package.

e) MCP6S22T-I/MS: Tape and Reel, Two Channel PGA, MSOP package.

f) MCP6S26-I/P: Six Channel PGA, PDIP package.

g) MCP6S26-I/SN: Six Channel PGA, SOIC package.

h) MCP6S26T-I/ST: Tape and Reel, Six Channel PGA, TSSOP package.

i) MCP6S28T-I/SL: Tape and Reel, Eight Channel PGA, SOIC package.

